TDA8947J / N2

4-channel audio amplifier
SE: 1 to 25W; BTL: 4 to 50W

Jun 04, 2003 **Final specification**

1. General description

The TDA8947J / N2 contains four identical audio power amplifiers. The TDA8947J / N2 can be used as four single ended (SE) channels with a fixed gain of 26 dB, two times bridge tied load (BTL) channels with a fixed gain of 32 dB or two times single ended (26 dB gain) and one bridge tied load (32 dB gain) channel for a 2.1 system.

The TDA8947J / N2 comes in a 17-pin Dil-Bent-Sil (DBS) power package. The TDA8947J / N2 is pin compatible with the TDA8944AJ / N2 and TDA8946AJ / N2.

The TDA8947J / N2 contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions and no unnecessary audio holes. Almost any supply voltag / load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

2. Features

- SE: 4 x 14W, BTL: 2 x 29W or SE: 2 x 14W and BTL: 1 x 29W opperation possibility (2.1 system)
- Soft clipping
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with the TDA8944AJ/N2 and TDA8946AJ/N2

3. Applications

- Television
- PC speakers
- Boom box
- Mini and micro audio receivers

PHILIPS

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	Operating	9	18	26	V
		No signal	-	-	28	V
I_q	quiescent supply current	V_{CC} = 18 V; R_L = ∞	-	100	145	mA
I_{stb}	standby supply current		-	-	10	µA
P_o	SE output power	THD = 10%; R_L = 4 Ω; V_{CC} = 18 V	7	8.5	-	W
		THD = 10%; R_L = 4 Ω; V_{CC} = 22 V	-	14	-	W
	BTL output power	THD = 10%; R_L = 8 Ω; V_{CC} = 18 V	16	18	-	W
		THD = 10%; R_L = 8 Ω; V_{CC} = 22 V	-	29	-	W
THD	total harmonic distortion	P_o = 1 W	-	0.05	0.5	%
$G_{v(max)}$	maximum voltage gain	S.E.	25	26	27	dB
		B.T.L.	31	32	33	dB
SVRR	supply voltage ripple rejection	B.T.L.; f = 1 kHz	-	65	-	dB
		S.E.; f = 1 kHz	-	60	-	dB

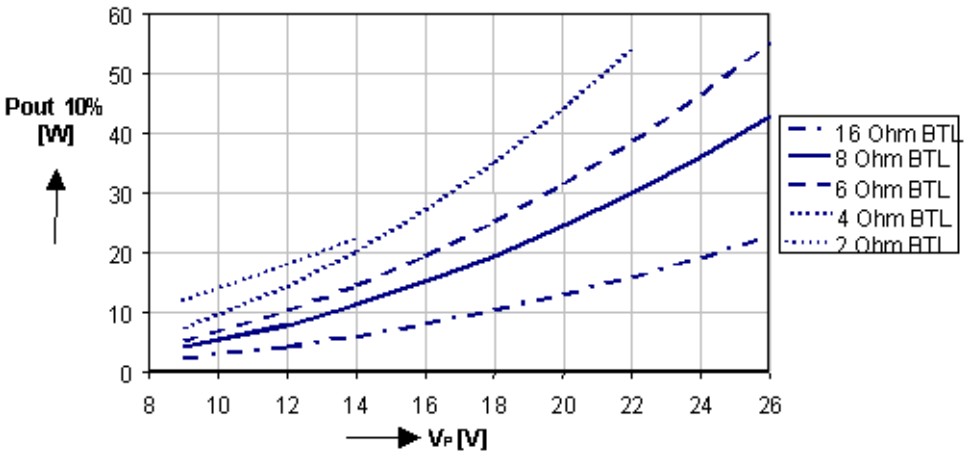


Fig 1. Output power (THD = 10%, one channel) versus supply voltage for various BTL loads.

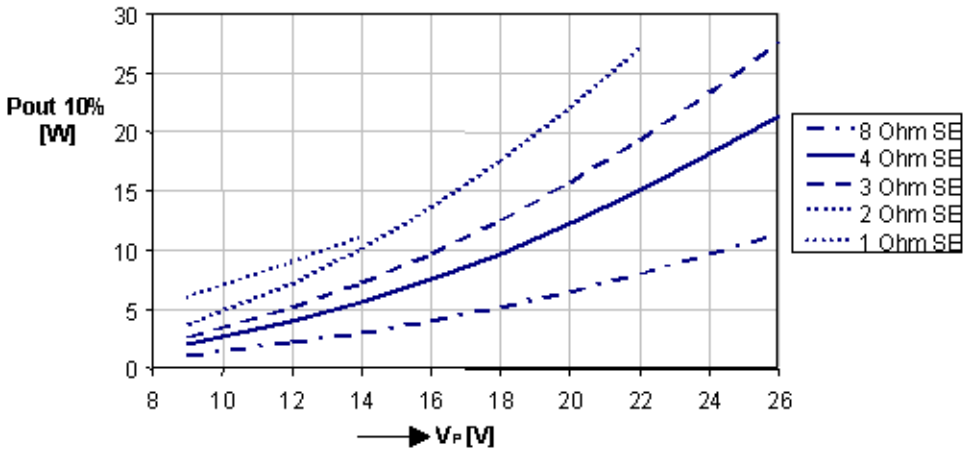


Fig 2. Output power (THD = 10%, one channel) versus supply voltage for various SE loads.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8947J / N2	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

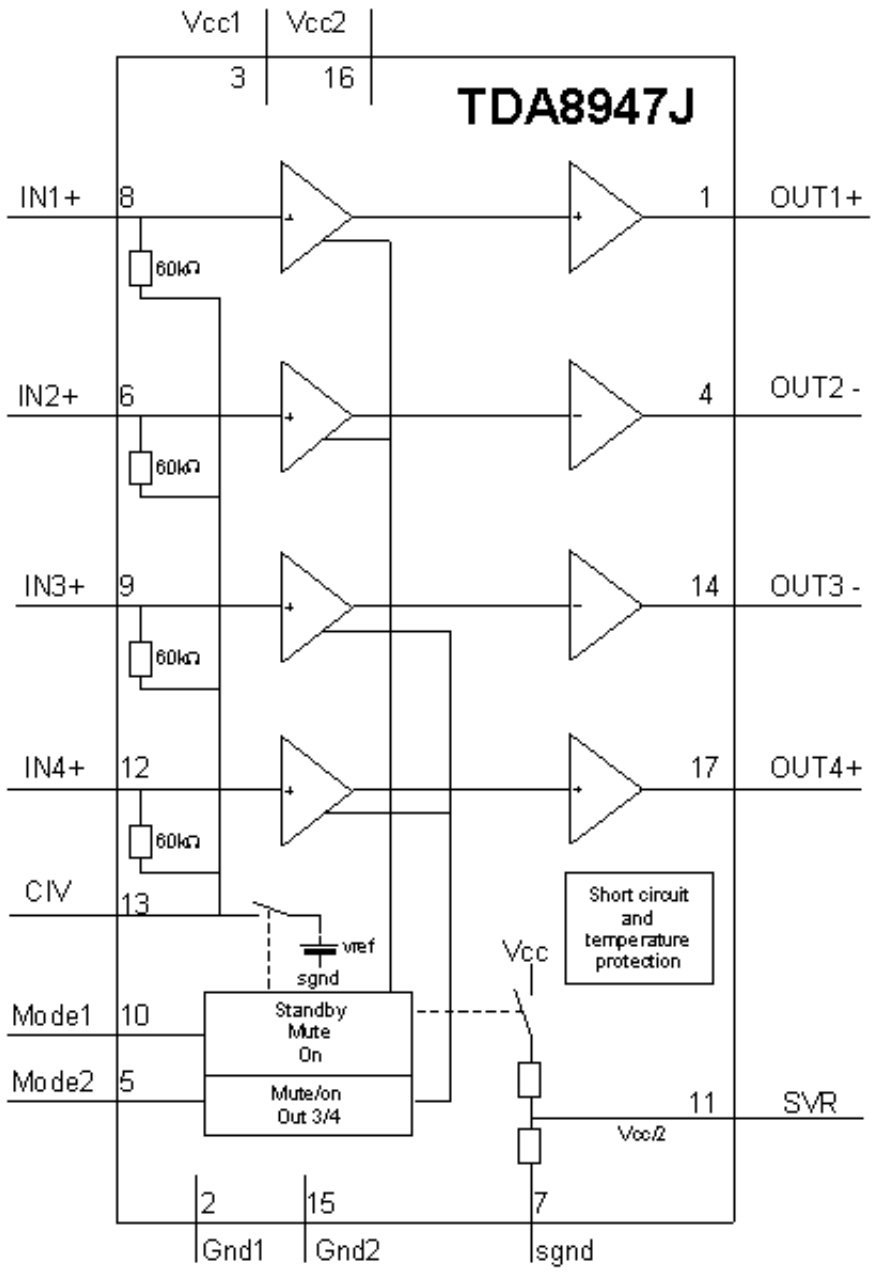


Fig 3. Block diagram.

7. Pinning information

7.1 Pinning

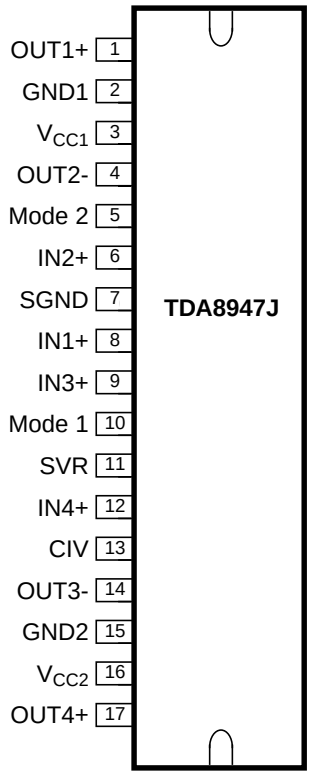


Fig 4. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OUT1+	1	non inverted loudspeaker terminal 1
GND1	2	ground channel 1
V_{CC1}	3	supply voltage channel 1
OUT2–	4	inverted loudspeaker terminal 2
Mode 2	5	mode selection of subwoofer (channel 3/4)
IN2+	6	input 2
SGND	7	signal ground
IN1+	8	input 1
IN3+	9	input 3
Mode 1	10	mode selection input (standby, mute, operating)
SVR	11	half supply voltage decoupling (ripple rejection)
IN4+	12	input 4

Table 3: Pin description...*continued*

Symbol	Pin	Description
CIV	13	Common input voltage decoupling
OUT3–	14	inverted loudspeaker terminal 3
GND2	15	ground channel 2
V_{CC2}	16	supply voltage channel 2
OUT4+	17	non inverted loudspeaker terminal 4

8. Functional description

8.1 Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)}$$

Single ended application, R_i= 60 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \cdot 10^{3} \times 220 \cdot 10^{-9})} = 12 \text{ Hz}$$

BTL application, R_i= 120 kΩ and C_i = 470 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(120 \cdot 10^{3} \times 470 \cdot 10^{-9})} = 2{,}8 \text{ Hz}$$

As shown in the formulaes above, large capacitors values for the inputs are not necessary; so the switch-on delay during charging of the input capacitors can be minimized. This result in a good low frequency response and good switch-on behaviour.

8.2 Power amplifier

The power amplifier is a Bridge Tied Load (BTL) and/or single ended (SE) amplifier with an all-NPN output stage, capable of delivering a peak output current of 4 A.

Using the TDA8947J / N2 as a BTL amplifier offers the following advantages:

- Lower peak value of the supply current
- The ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking output capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%; see figure 11a. The maximum output power is limited by the supply voltage of 26V and the maximum available output current; 4 A repetitive peak current. A minimum load (BTL) of 8Ω is allowed at supply voltages above 22V.

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom - compared to the average power output - for transferring the loudest parts without distortion. At V_{CC} = 18 V and P_o = 10 W (BTL with R_L = 8Ω) or P_o = 5 W (SE with R_L = 4Ω) at THD = 0.2 %(see figure 7a), the Average Listening Level (ALL) - music power - without any distortion yields:

$$P_{O(AL(L,\,BTL))} = \frac{10\ \text{W}}{15.85} = 630\ \text{mW}$$

$$P_{O(AL(L,\,SE))} = \frac{5\ \text{W}}{15.85} = 315\ \text{mW}$$

The power dissipation can be derived from figure 15a for 0 dB respectively 12 dB headroom.

Table 4: Power rating as function of headroom

Headroom	Power output (THD = 0.2 %)		Total power dissipation
	BTL	SE	All channels driven
0 dB	Po = 10 W	Po = 5 W	Pdiss = 18 W
12 dB	Po(ALL) = 630 mW	Po = 315 mW	Pdiss = 9 W

For the average listening level a power dissipation of 9 W can be used for a heatsink calculation.

8.3 Mode selection

The TDA8947J / N2 has three functional modes, which can be selected by applying the proper DC voltage to pin MODE 1. Output 3 and 4 can be switched on/off by a proper DC-voltage to pin MODE 2, at on-mode of output 1 and 2. A typical application diagram is given in figure 19.

Table 5: Mode selection

Mode 1	Mode 2	Amp 1,2	Amp 3,4 Subwoofer
0 - 0.8V	0 - V_{cc}	Standby	
4.5 - (V_{cc}-3.5V)	0 - V_{cc}	Mute	
(V_{cc}-2.0V) - V_{cc}	0 - (V_{cc} - 3.5V)	On	Mute
	(V_{cc}-2V) - V_{cc}	On	On

Standby — In this mode the current consumption is very low and the outputs are floating. The device is in standby mode when V_{MODE1} < 0.8 V, or when the MODE1 pin is grounded. In standby the second channel function (mode 2) has been disabled.

Mute — In this mode the amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when 4.5 V < V_{MODE1} < (V_{CC} – 3.5 V).

Operating — In this mode the amplifier is operating normally. The operating mode is activated at V_{MODE1} > V_{CC} - 2 V. Output 3 and 4 can be set to mute or operating.

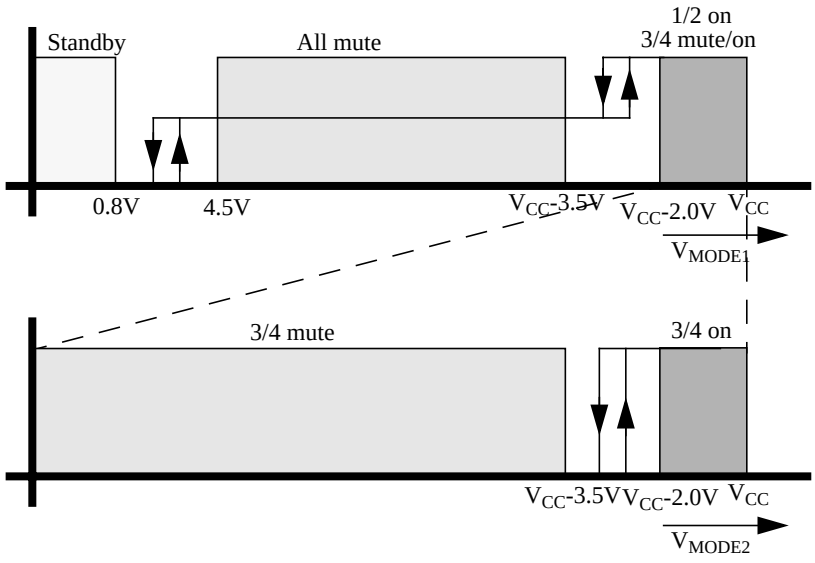


Fig 5. Mode selection.

8.3.1 Switch-on and switch off

T.B.F.

8.4 Supply voltage Ripple Rejection (SVRR)

The SVRR is measured with an electrolytic capacitor of 150uF on pin SVR using a bandwidth of 10Hz to 22kHz, figure 17 illustrates the SVRR as function of the frequency. A larger capacitor value on the SVR pin improves the ripple rejection behavior at the lower frequencies.

8.5 Built-in protection circuits

The TDA8944AJ contains two types of detection sensors; one measures local temperatures of the power stages and one the global chip temperature. At a local temperature of approx. 220 ºC or a global temperature of approx. 150 ºC this detection circuit switches off the power stages for 3,5 mSec. High impedance of the outputs is the result. After this time period the power stages switches on automatically and the detection will take place again; still a too high temperature switches off the power stages immediately. This protects the TDA8944AJ against shorts to ground, to the supply voltage, across the load and too high chip temperatures.

The protection will only be activated when necessery, so even during a short circuit condition, a certain amount of (pulsed) current will still be flowing through the short, just as much as the power can handle without exceeding the critical temperature level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	no signal	–0.3	+28	V
V_{CC}	supply voltage	operating	-0.3	+26	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	4	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
P_{tot}	total power dissipation		-	69	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection		-	24	V

10. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	all channels driven	1.8	K/W

11. Static characteristics

Table 8: Static characteristics

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE1} = V_{CC} V; V_{MODE2} = V_{CC}; V_i = 0 V; measured in test circuit Figure 19; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC} [1]	supply voltage	operating		9	18	26	V
I_q	quiescent supply current	R_L = ∞	[2]	-	100	145	mA
I_{stb}	standby supply current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	DC output voltage		[3]	-	9	-	V
ΔV_{OUT} [4]	differential output voltage offset	BTL mode		-	-	170	mV
$V_{MODE\ 1}$	mode 1 selection input voltage	operating mode 1		V_{CC} - 2.0	-	V_{CC}	V
		mute mode 1		4.5	-	V_{CC} – 3.5	V
		standby mode 1		0	-	0.8	V
$V_{MODE\ 2}$ [5]	mode 2 selection input voltage	operating mode 2	[4]	V_{CC} - 2.0	-	V_{CC}	V
		mute mode 2		0	-	V_{CC} – 3.5	V
I_{MODE1}	mode 1 selection input current	0 < V_{MODE1} < V_{CC}		-	-	20	µA
I_{MODE2}	mode 2 selection input current	0 < V_{MODE2} < V_{CC}		-	-	20	µA

[1] A minimum load (BTL) of 8Ω is allowed at supply voltages above 22V.
[2] With a load connected at the outputs the quiescent current will increase.
[3] The DC output voltage with respect to ground is approximately 0.5V_{CC}.
[4] $\Delta V_{OUT} = |V_{OUT+} - V_{OUT-}|$.

[5] Channel 3 and 4 can only be set to mute or operating by V_{MODE2} when $V_{MODE1} > V_{CC}$-2,5V.

12. Dynamic characteristics

Table 9: Dynamic characteristics BTL

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 19; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 8 ohm		16	18	-	W
		THD = 0.5%; R_L = 8 ohm		-	14		W
		V_{CC} = 22V; THD = 10%; R_L = 8 ohm			29		W
THD	total harmonic distortion	P_o = 1 W		-	0.05	0.5	%
G_v	B.T.L. voltage gain			31	32	33	dB
$Z_{i(dif)}$	differential input impedance			75	120	-	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	200		μV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	65	-	dB
$V_{o(mute)}$	output voltage	mute mode	[3]			250	μV
α_{cs}	channel separation	R_{source} = 0 ohm		50	65	-	dB
$\|G_v\|$	channel unbalance					1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with a mode 1 and mode 2 voltage of 7 V and an input voltage of 1 V (RMS) in a bandwidth from 20Hz to 22 kHz, so including noise.

Table 10: Dynamic characteristics SE

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 19; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 4 ohm		7	8.5	-	W
		THD = 0.5% R_L = 4 ohm		-	6.5	-	W
		V_{CC} = 22V; THD = 10%; R_L = 4ohm			14		W
THD	total harmonic distortion	P_o = 1 W		-	0.1	0.5	%
G_v	S.E. voltage gain			25	26	27	dB
$Z_{i(dif)}$	differential input impedance			40	60	-	kΩ
$V_{n(o)}$	noise output voltage		[1]		150		μV

Table 10: Dynamic characteristics SE…*continued*

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 19; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	60	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	60	-	dB
$V_{o(mute)}$	output voltage	mute mode	[3]			150	μV
α_{cs}	channel separation	R_{source} = 0 ohm		50	60	-	dB
$\|G_v\|$	channel unbalance					1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with a mode 1 and mode 2 voltage of 7 V and an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, so including noise.

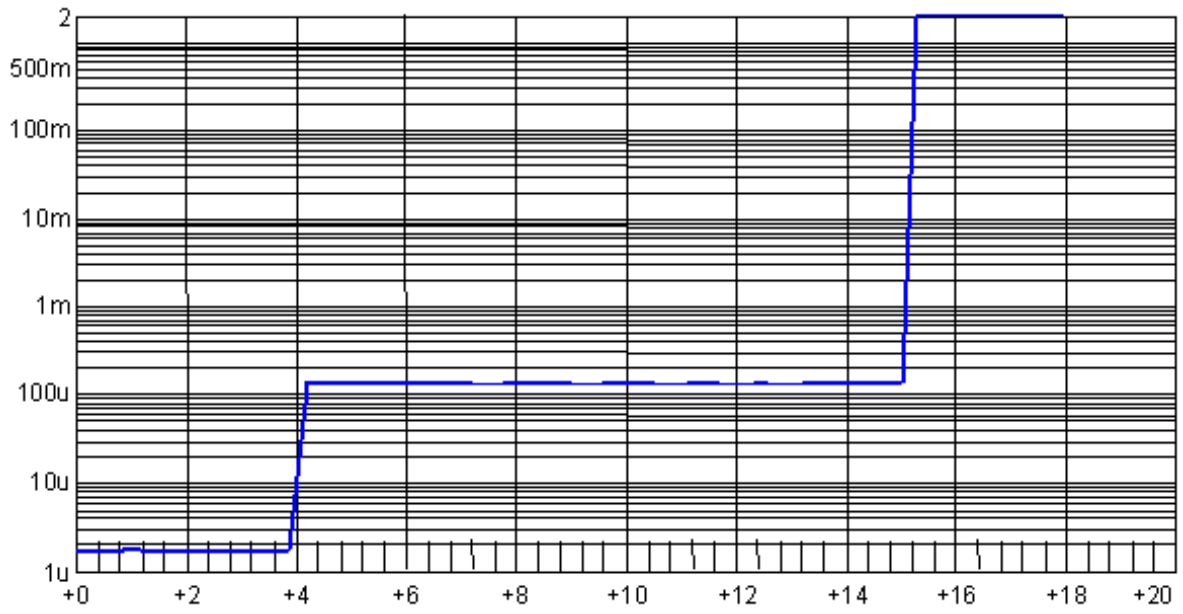


Fig 6. AC output voltage as function of mode voltage. V_{in} = 50 mV B.T.L.; V_{CC} = 18 V

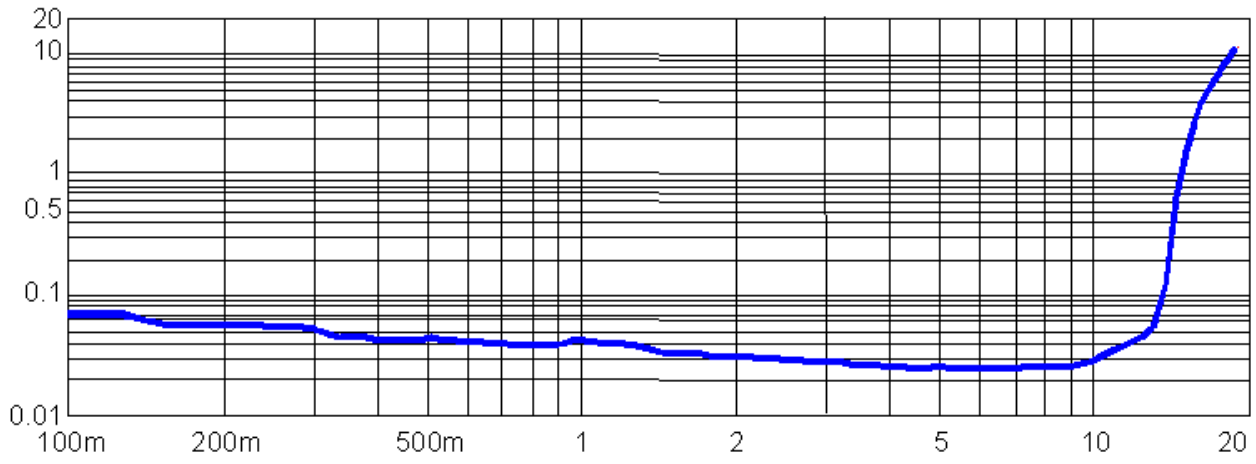


Fig 7. Total harmonic distortion as a function of output power B.T.L.; V_{CC} = 18V; f = 1kHz; R_L = 8Ω.

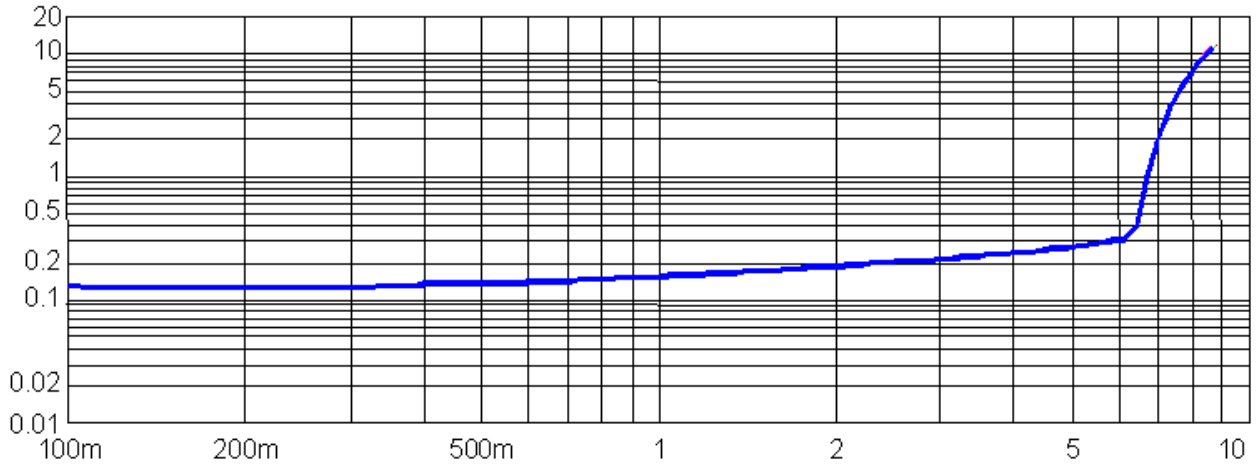


Fig 8. Total harmonic distortion as a function of output power S.E.; V_{CC} = 18V; f = 1kHz; R_L = 4Ω.

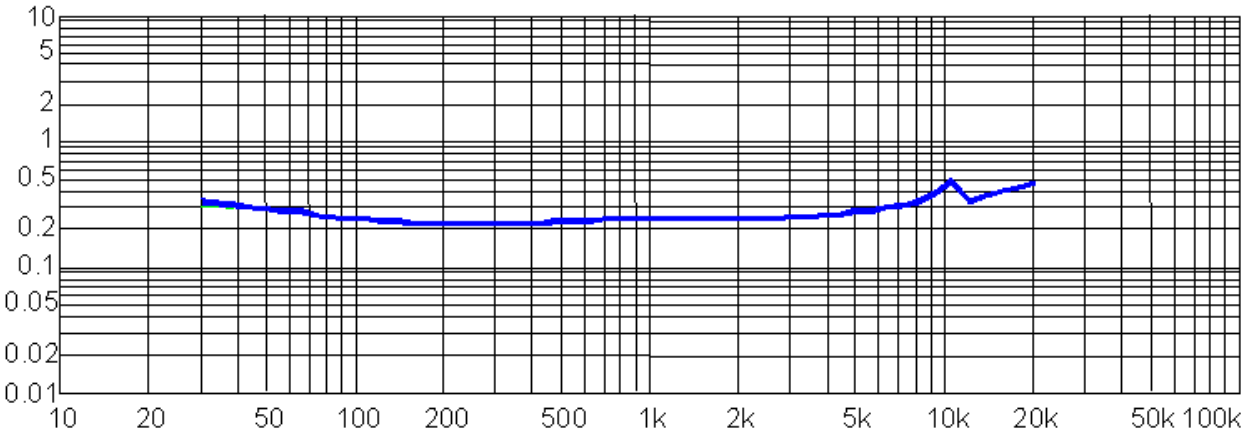


Fig 9. Total harmonic distortion as a function of frequency S.E.; V_{CC} = 18V, Po = 1W; R_L = 4Ω.

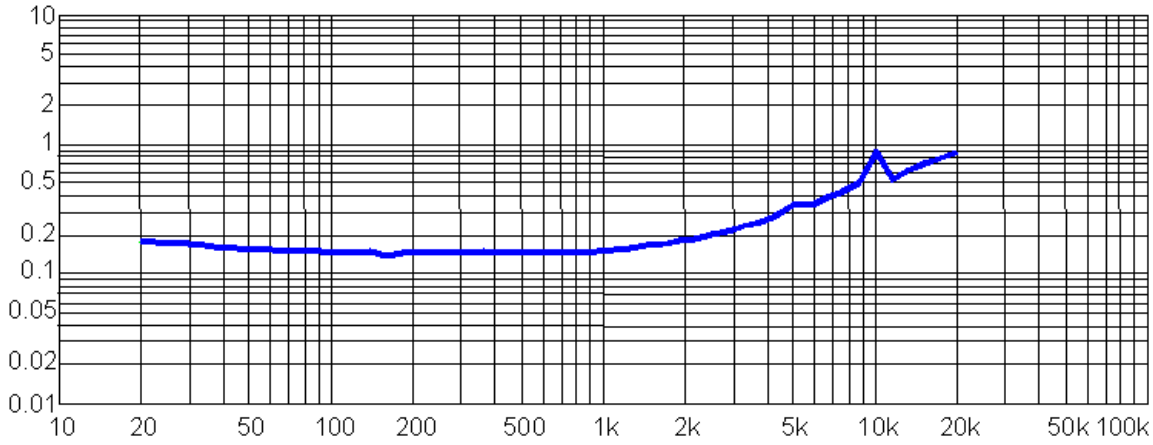


Fig 10. Total harmonic distortion as a function of frequency B.T.L.; V_{CC} = 18V, Po = 1W; R_L = 8Ω.

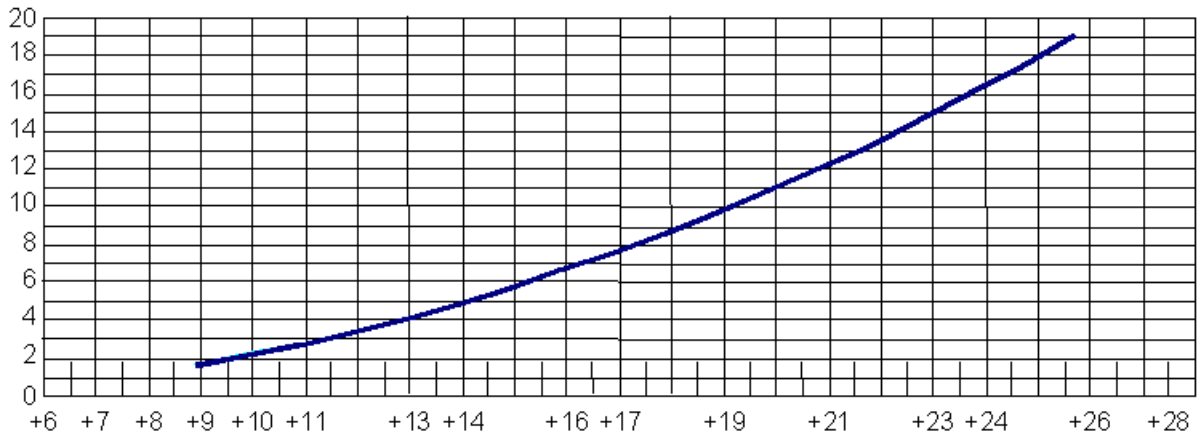


Fig 11. Output power as function of supply voltage at THD = 10%, S.E., R_L = 4Ω; f = 1kHz.

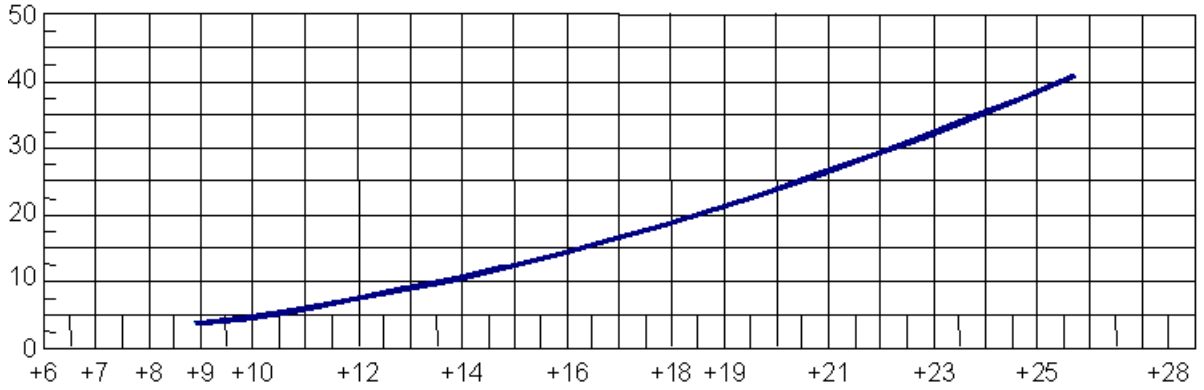


Fig 12. Output power as function of supply voltage at THD = 10%, B.T.L., R_L = 8 Ω; f = 1kHz.

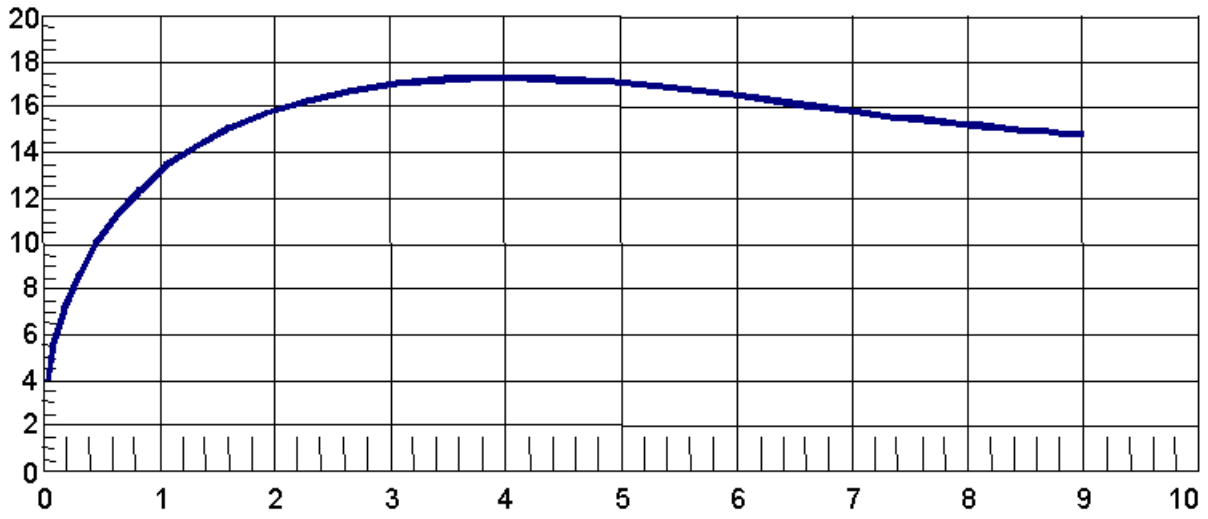


Fig 13. Total (worst case, all channels driven) power dissipation as function of channel output power per channel, S.E.; V_{CC} = 18V; R_L = 4Ω.

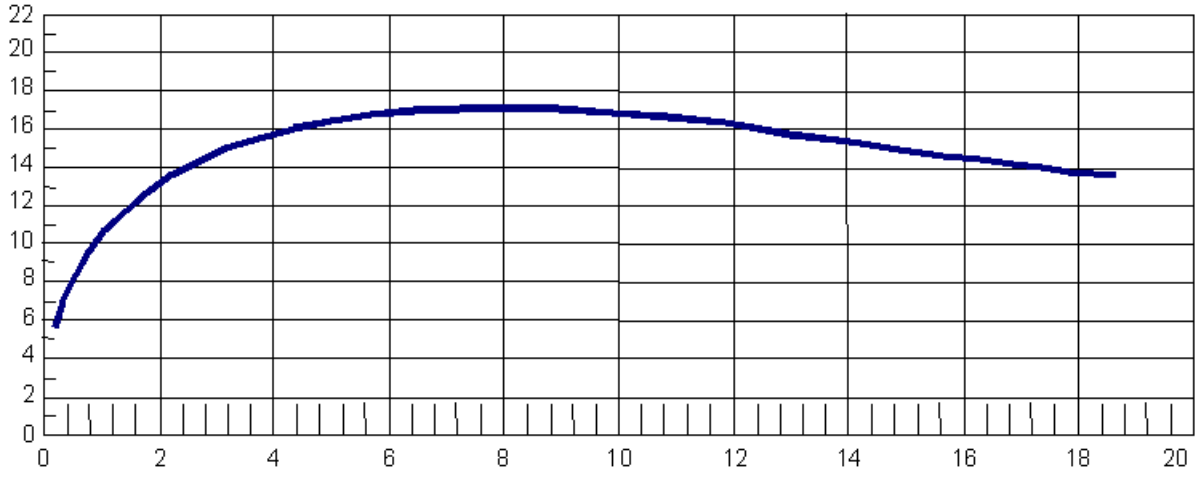


Fig 14. Total (worst case, all channels driven) power dissipation as function of channel output power per channel, B.T.L.; V_{CC} = 18V; R_L = 8Ω.

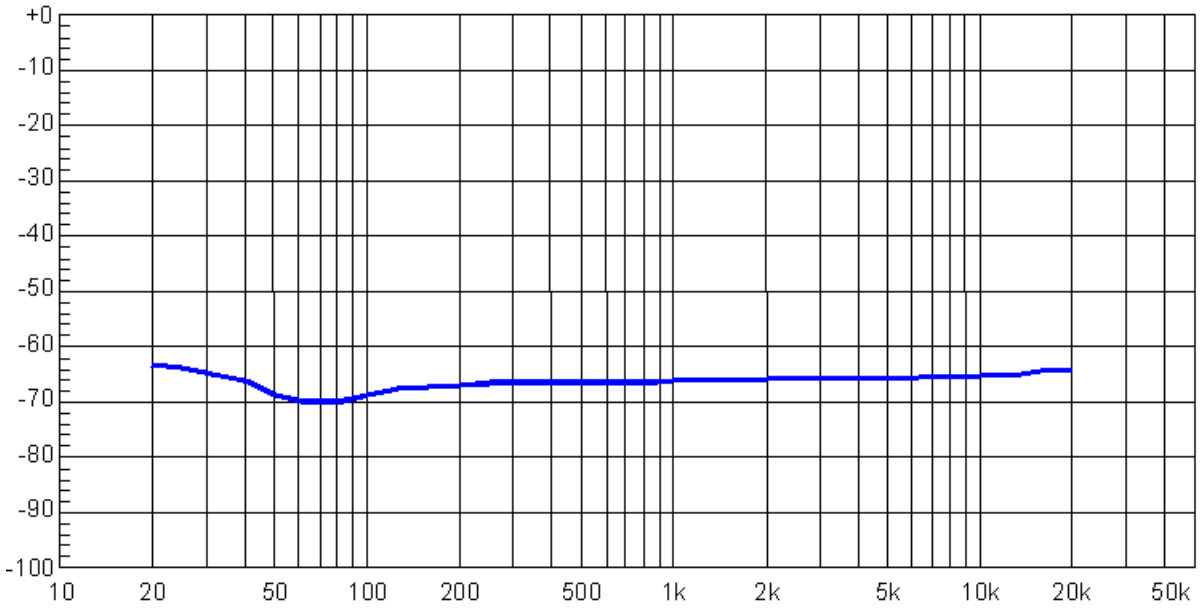


Fig 15. Channel seperation as function of frequency (no bandpass filter applied), S.E., V_{CC} = 18 V; R_L = 4Ω.

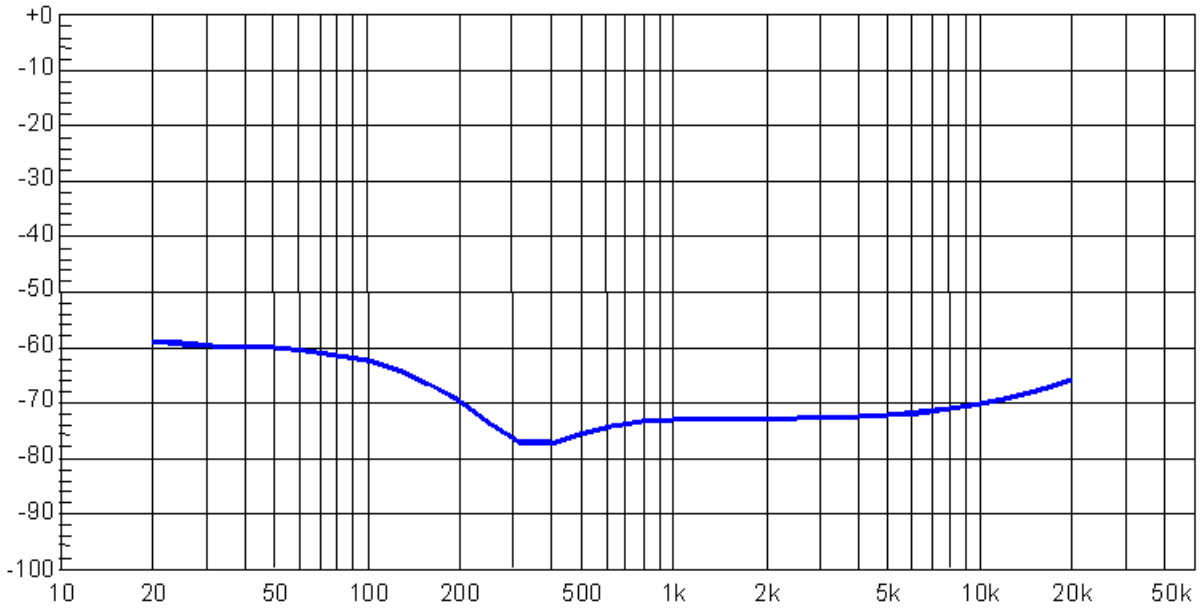
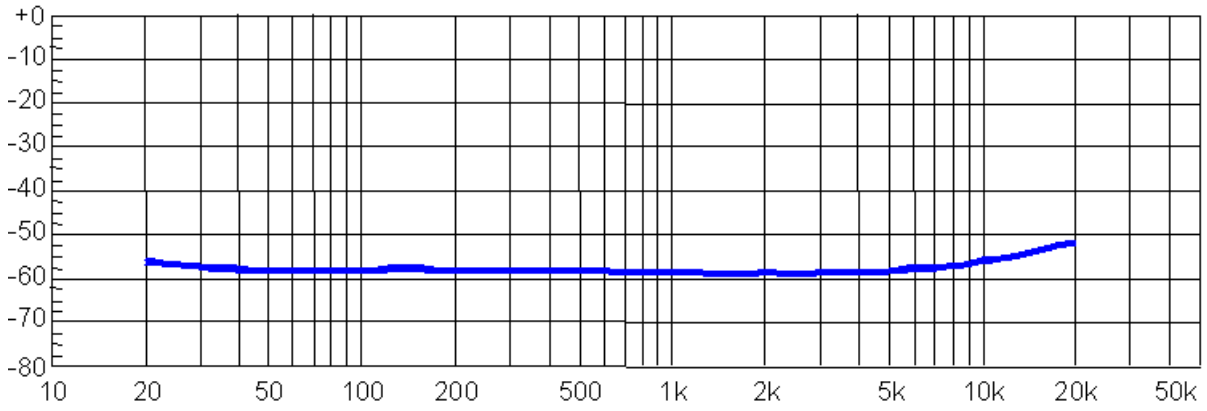
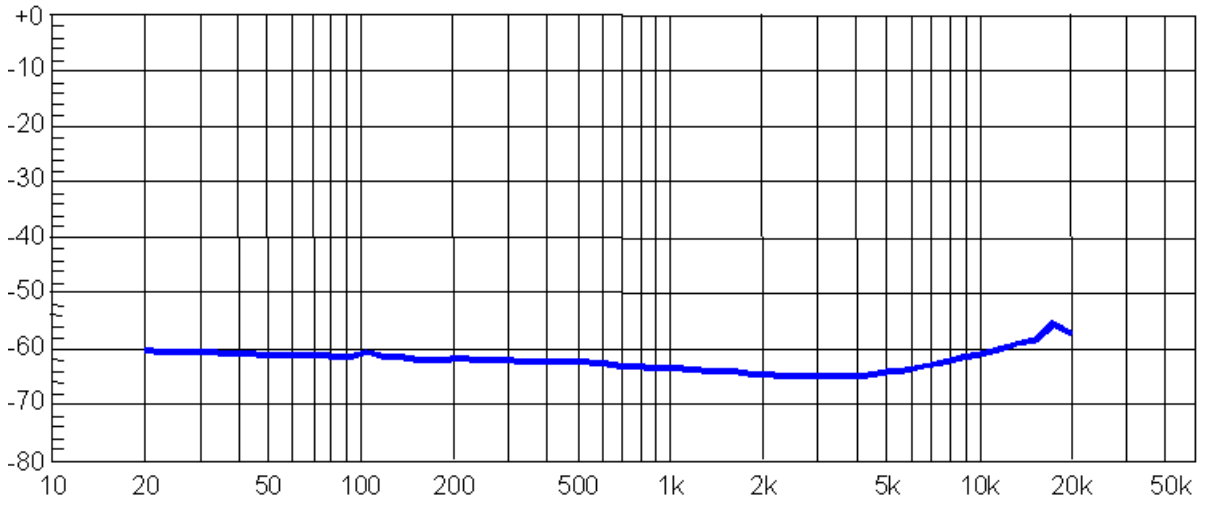


Fig 16. Channel separation as function of frequency (no bandpass filter applied), B.T.L., V_{CC} = 18 V



V_{CC} = 18 V, R_S = 0 Ω; V_{ripple} = 300mV (RMS); A bandpass filter of 20 Hz to 22 kHz ahs been applied. Inputs short circuited.

Fig 17. Supply voltage ripple rejection as function of frequency, S.E.



V_{CC} = 18 V, R_S = 0 Ω; V_{ripple} = 300mV (RMS); A bandpass filter of 20 Hz to 22 kHz ahs been applied. Inputs short circuited.

Fig 18. Supply voltage ripple rejection as function of frequency, B.T.L.

13. Application information

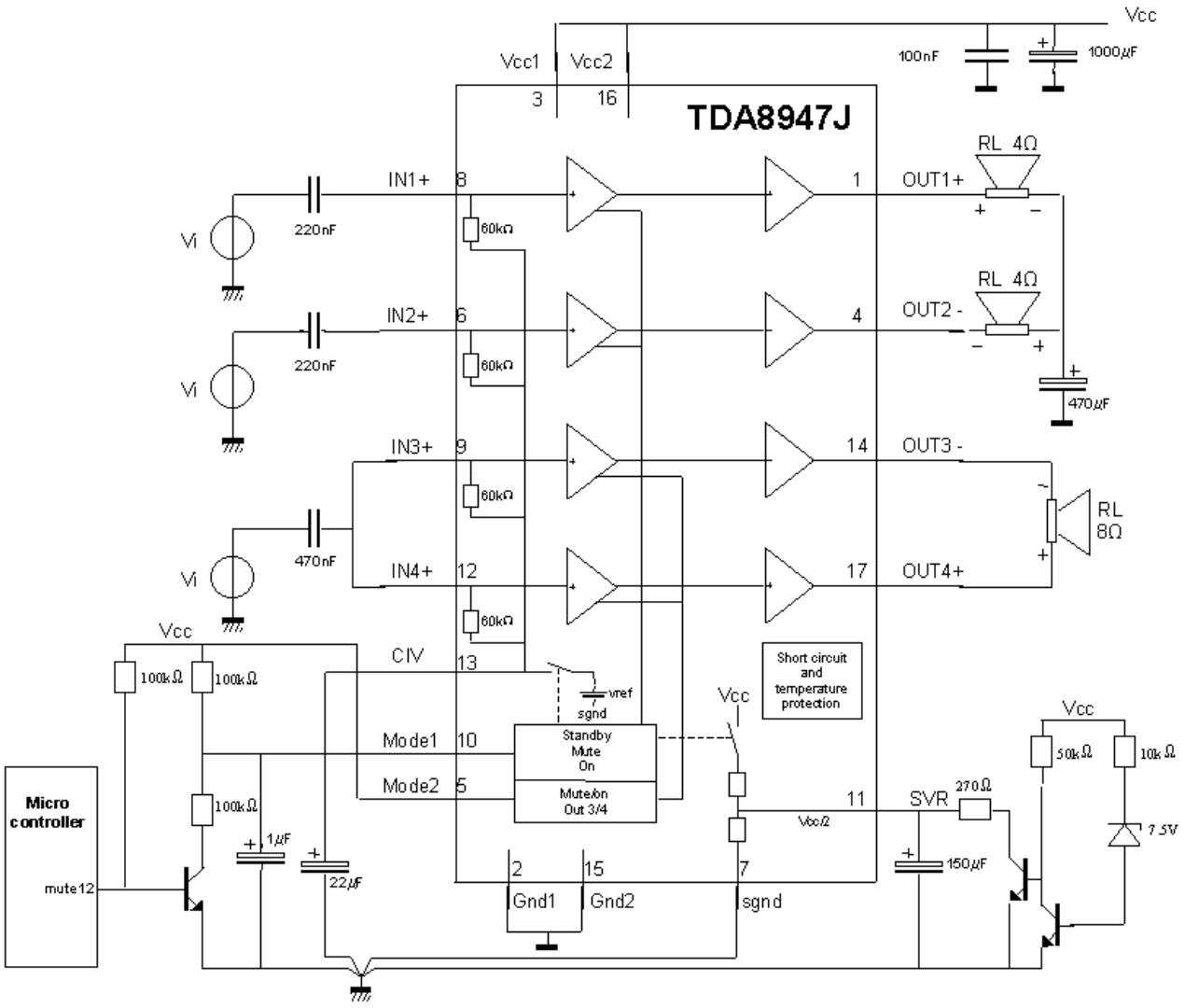


Fig 19. Typical application diagram.

Note: Switching inductive loads, the output voltage can rise beyond the maximum product voltage of 28V. At high supply voltage it is recommended to use (shottky) diodes to the supply voltage and ground.

Table 11: Amplifier selection by microcontroller (open collector outputs)

Microcontroller			Amplifier	
on/off	mute12	mute34	Out1+ & Out2-	Out3- & Out4+
low	low	low	Operational	Operational
low	low	high	Operational	Mute
low	high	don't care	Mute	Mute
high	don't care	don't care	Standby	

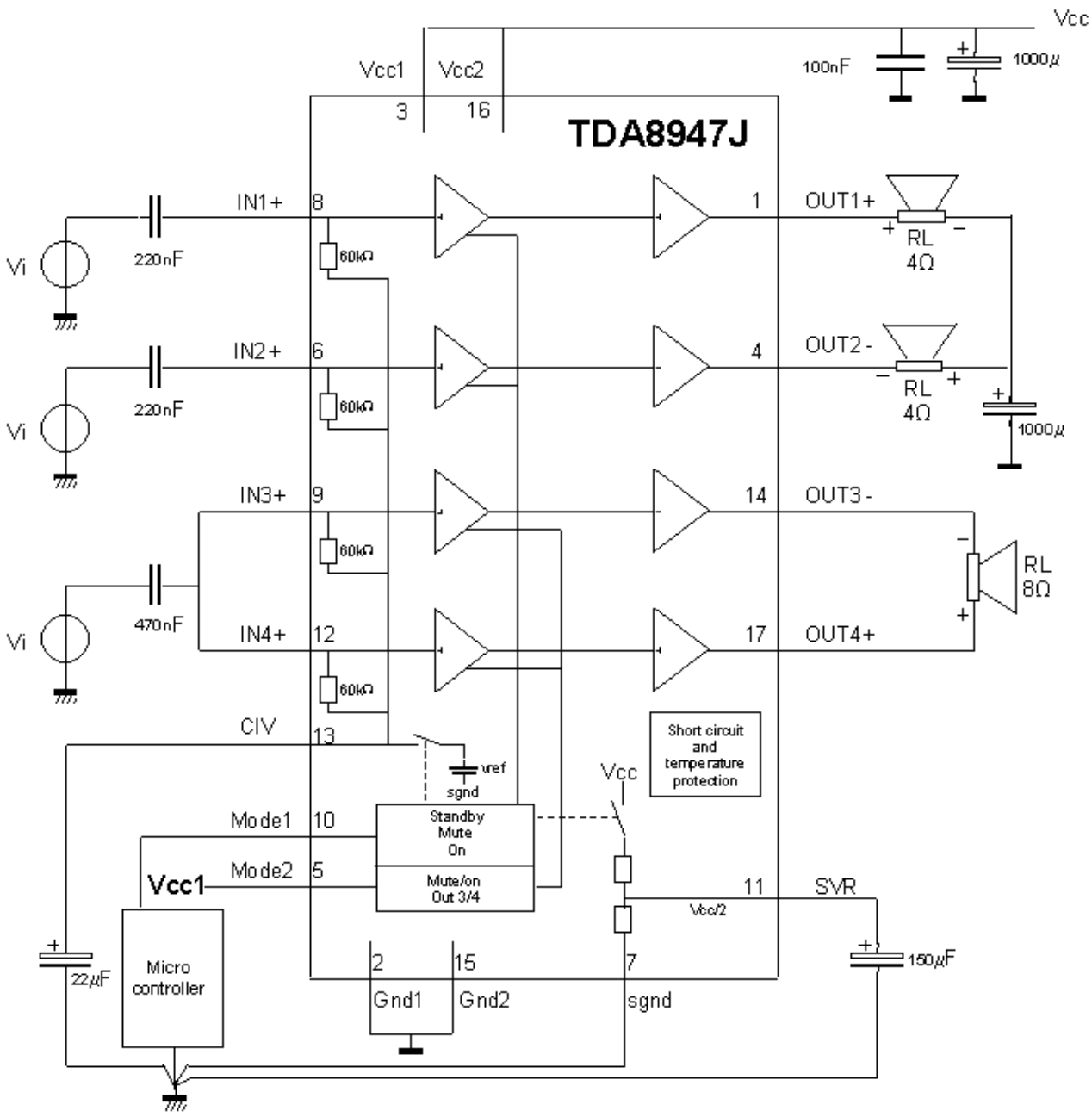


Fig 20. Application diagram, one pin control and reduction of capacitor.

Note: Mode 2 has been connected to the supply pin, e.g. pin 3 which is just beside. The loads of outputs 1 and 2 are connected to one capacitor.

13.1 Printed-circuit board

13.1.1 Layout and grounding

To obtain a high level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

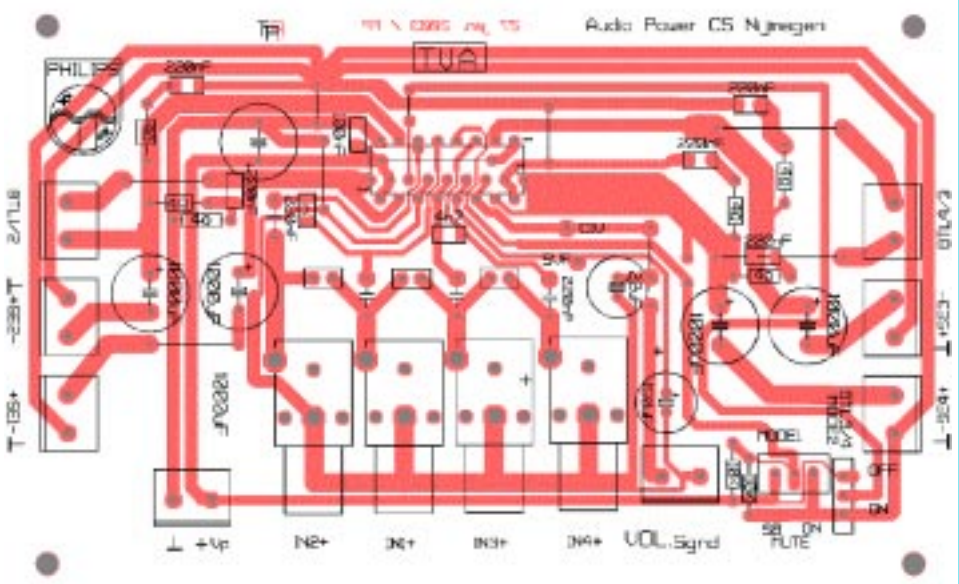


Fig 21.Printed-circuit board layout (single-sided); components view.

13.1.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR - typical 100nF - has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor - e.g. 1000uF or greater - must be placed close to the device.

The bypass capacitor on the SVR pin reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

13.2 Thermal behaviour and heatsink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j\text{-}mb)}$ is 1.8 K/W. A calculation for the heatsink can be made, with the following parameters:

$T_{amb(max)}$ = 60 °C

V_{CC} = 18 V and R_L = 8 Ω

$T_{j(max)}$ = 150 °C

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heatsink. In the heatsink calculations the value of $R_{th(mb-h)}$ is ignored.

At V_{CC} = 18 V and R_L = 8 Ω (4 times S.E.) the measured worst-case sine-wave dissipation is 17 W; see figure 13. For $T_{J(max)}$ = 150 °C the temperature raise - caused by the power dissipation - is: 150 - 60 = 90 °C.

P x $R_{th(tot)}$ = 90 °C

$R_{th(tot)}$ = 90 / 17 = 5.29 K/W

$R_{th(h-a)}$ = $R_{th(tot)}$ - $R_{th(j-mb)}$ = 5.29 - 1.8 = 3.49 K/W

The calculation above is for an application at wordt-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see Section 8.2.2). This allows for the use of smaller heatsink:

P x $R_{th(tot)}$ = 90 °C

$R_{th(tot)}$ = 90 / 8.5 = 9.41 K/W

$R_{th(h-a)}$ = $R_{th(tot)}$ - $R_{th(j-mb)}$ = 9.41 - 1.8 = 7.61 K/W

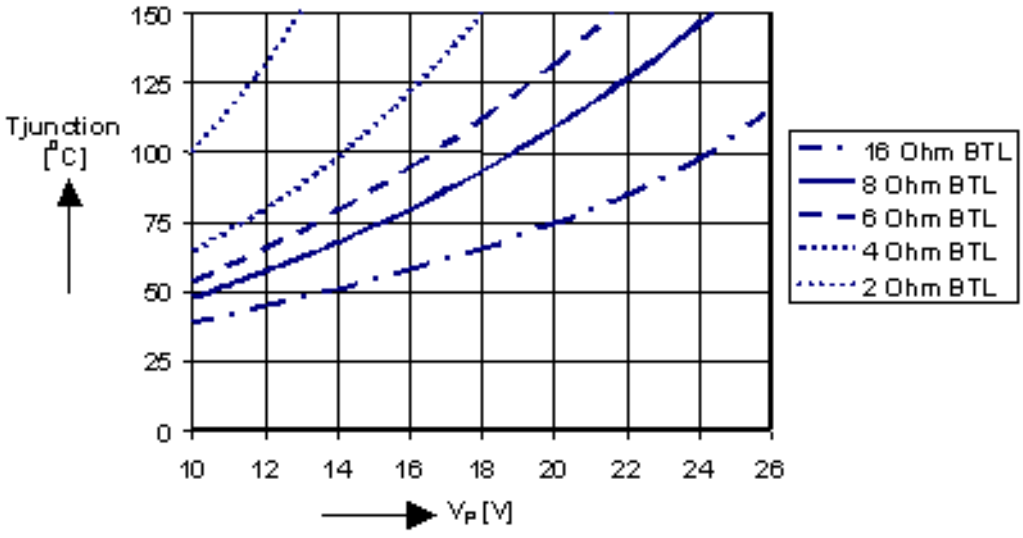


Fig 22.Junction temperature with music signals versus supply voltage for various 2 * BTL loads for Tambient = 25°C and an external heatsink of 5 K/W.

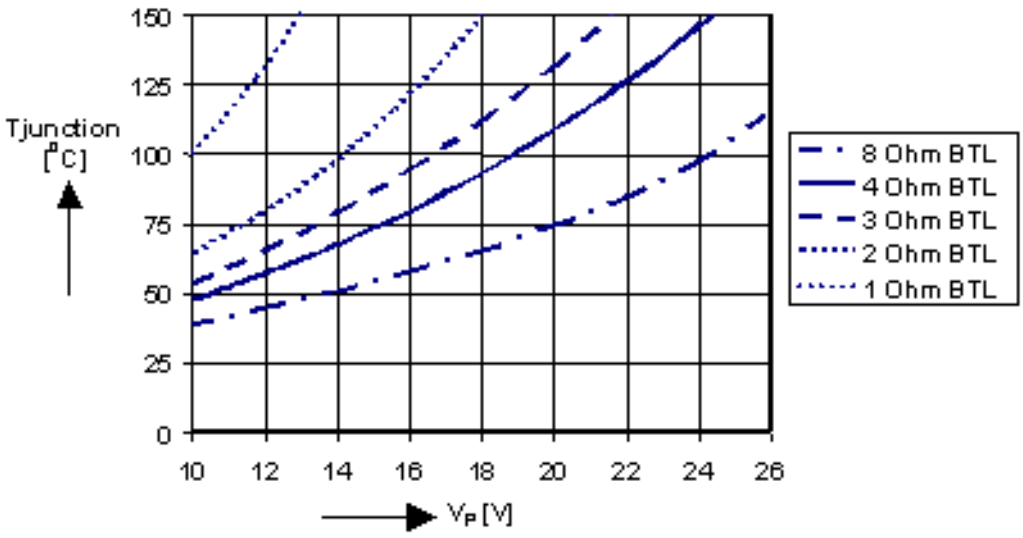


Fig 23.Junction temperature with music signals versus supply voltage fro various 4 * SE loads for Tambient = 25^{O}C and an external heatsink of 5 K/W.

14. Test information

14.1 Quality information

The *"General Quality Specification for Integrated Circuits, SNW-FQ-611-part D"* is applicable and reference can be found in the *"Quality Reference Handbook, chapter Quality standards for customers"*. The handbook can be ordered using the code 9397 750 02391.

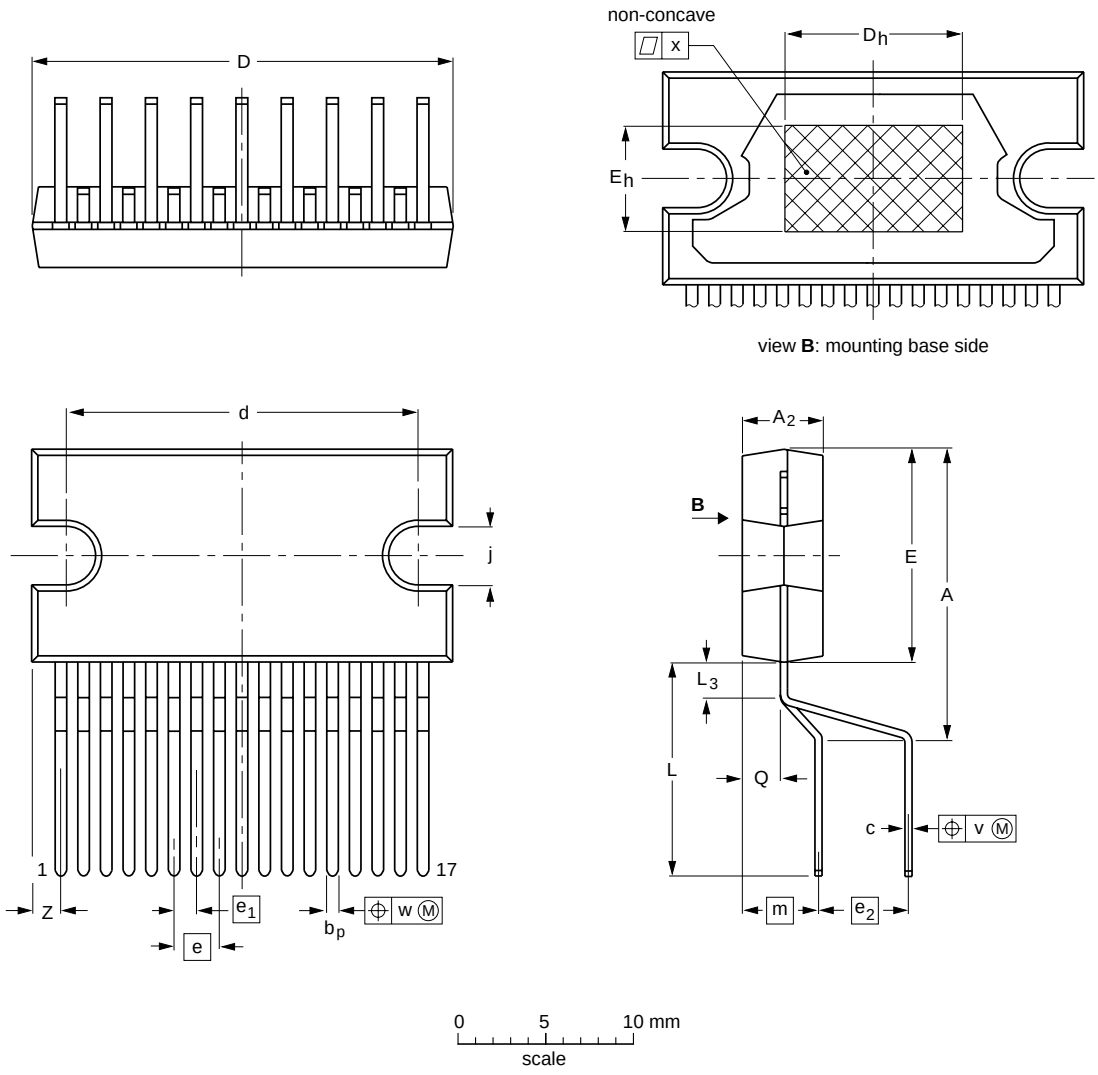
14.2 Test conditions

T_{amb} = 25 ^{o}C; V_{CC} = 18 V; f = 1 kHz; R_L = 8 Ω; audio pass band 22 Hz to 22 kHz; unless otherwise specified.

Remark: In the graphs as function of frequency no bandpass filter was applied; see figure 7b and 15b.

15. Package outline

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~95-03-11~~ 97-12-16

Fig 24. DBS17P package outline.

16. Soldering

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Package related soldering information

Table 12: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable [1]

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.