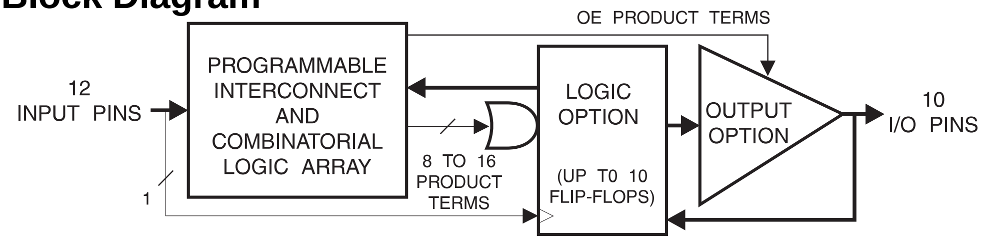
Features

- 3.0V to 5.5V Operating Range
- Advanced Low Voltage Electricaly Erasable Programmable Logic Device
- User Controlled Power Down Pin Option
- Pin-Controlled Standby Power (10 µA Typical)
- Well-Suited for Battery Powered Systems
- 10 ns Maximum Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
- Latch Feature Hold Inputs to Previous Logic States
- Advanced Electrically Erasable Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance E² PLD

ATF22LV10C

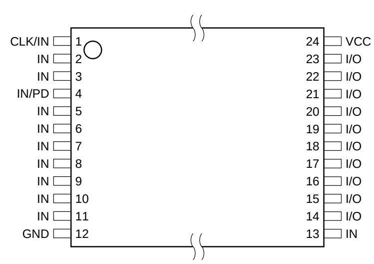
Block Diagram



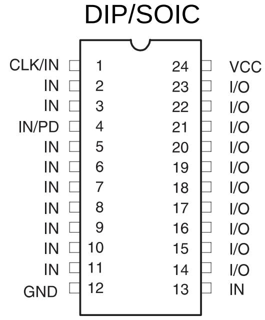
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
V_{CC}	(3V to 5.5V) Supply
PD	Programmable Power Down

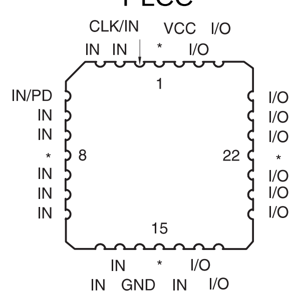
TSSOP Top View



DIP/SOIC



PLCC (1)



Top view

Note: 1. For PLCC, pin 1, 8, 15, and 22 can be left unconnected. For superior performance, connect V_{CC} to pin 1 and GND to 8, 15, and 22.

Rev. 0780E/LV10C-E–05/98

Description

The ATF22LV10C is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the 3.0V to 5.5V range for industrial and commercial temperature ranges.

The ATF22LV10C provides a low voltage and user controlled "zero" power CMOS PLD solution. A user-controlled power down feature offers "zero" (5 µA typical) standby power. This feature allows the user to manage total system power to meet specific application requirements and enhance reliability, all without sacrificing speed. (The ATF22LV10CZ provides edge-sensing "zero" standby power (10 µA typical), as well as low voltage operation. See the ATF22LV10CZ Data Sheet.)

The ATF22LV10C is capable of operating at supply voltages down to 3.0V. When the power down pin is active, the device is placed into a zero standby power down mode. When the power down pin is not used or active, the device operates in a full power low voltage mode. Pin "keeper" circuits on input and output pins hold pins to their previous logic levels when idle, which eliminate static power consumed by pull-up resistors.

The ATF22LV10C macrocell incorporates a variable product term architecture. Each output is allocated from 8 to 16 product terms which allows highly complex logic functions to be realized. Two additional product terms are included to provide synchronous reset and asynchronous reset. These additional product terms are common to all 10 registers and are automatically cleared upon power up. Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V (1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75V dc, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0V - 5.5V	3.0V - 5.5V

Functional Logic Diagram Description

The Functional Logic Diagram describes the ATF22LV10C architecture.

The ATF22LV10C has 12 inputs and 10 I/O macrocells. Each macrocell can be configured into one of four output configurations: active high/low, registered/combinatorial output. The universal architecture of the ATF22LV10C can be programmed to emulate most 24-pin PAL devices.

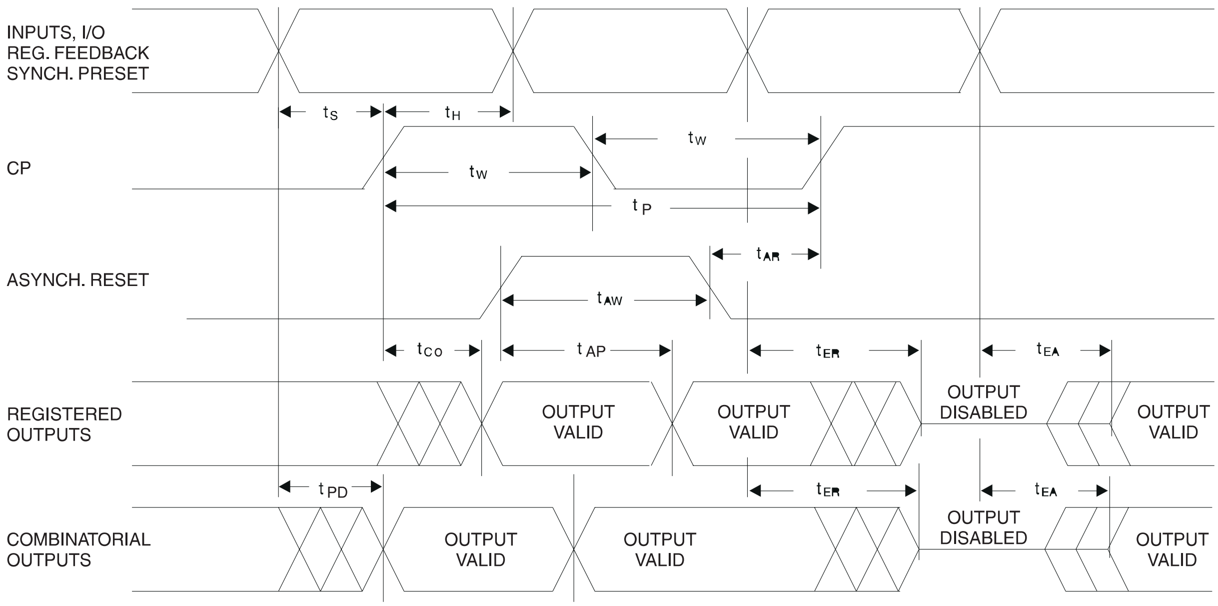
Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF22LV10C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

DC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}(max)$				-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$				10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	Com. Ind.		55 60	85 90	mA mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	Com. Ind.		1 1		mA/MHz mA/MHz
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f = 15 MHz	Com. Ind.			100 105	mA mA
I_{PD}	Power Supply Current, PD Mode	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	Com. Ind.		10 10	100 100	µA µA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V				-130	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OL} = 8 mA				0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN, I_{OH} = -4.0 mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

AC Waveforms



AC Characteristics [1]

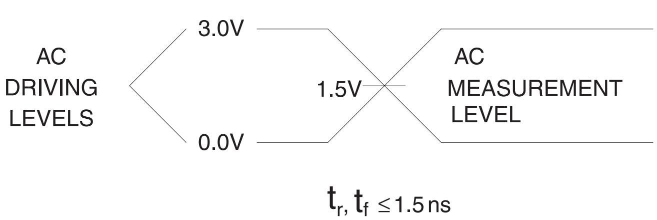
Symbol	Parameter	-10 Min	-10 Max	-15 Min	-15 Max	Units
t_{PD}	Input to Feedback to Non-Registered Output	3	10	3	15	ns
t_{CF}	Clock to Feedback		5		8	ns
t_{CO}	Clock to Output	2	6.5	2	10	ns
t_S	Input or Feedback Setup Time	7.5		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$ Internal Feedback $1/(t_S + t_{CF})$ No Feedback $1/(t_P)$		71.4 80 83.3		45.5 50 62.5	MHz MHz MHz
t_{EA}	Input to Output Enable	3	12	3	15	ns
t_{ER}	Input to Output Disable	2	12	2	15	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3	13	3	15	ns
t_{SP}	Setup Time, Synchronous Preset	10		10		ns
t_{AW}	Asynchronous Reset Width	8		8		ns
t_{AR}	Asynchronous Reset Recovery Time	6		6		ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	10		10		ns

Note: 1. See ordering information for valid part numbers.

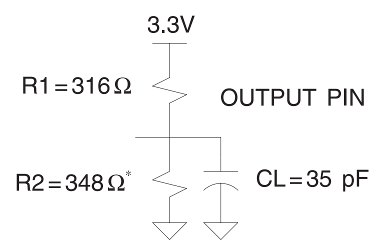
Power Down AC Characteristics

Symbol	Parameter	-10		-15		Units
		MIn	Max	Min	Max	
t_{IVDH}	Valid Input Before PD High	10		15		ns
t_{GVDH}	Valid OE Before PD High	0		0		ns
t_{CVDH}	Valid Clock Before PD High	0		0		ns
t_{DHIX}	Input Don't Care After PD High		10		15	ns
t_{DHGX}	OE Don't Care After PD High		10		15	ns
t_{DHCX}	Clock Don't Care After PD High		10		15	ns
t_{DLIV}	PD Low to Valid Input		5		7.5	ns
t_{DLGV}	PD Low to Valid OE		3		3	ns
t_{DLCV}	PD Low to Valid Clock		10		10	ns
t_{DLOV}	PD Low to Valid Output		7.5		7.5	ns

Input Test Waveforms and Measurement Levels



Output Test Loads



Note: Similar competitors' devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible device specification conditions.

Pin Capacitance (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF22LV10C are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic and start below 0.7V.

2. The clock must remain stable during T_{PR}.

3. After T_{PR}, all input and feedback setup times must be met before driving the clock pin high.

Preload of Register Outputs

The ATF22LV10C's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22LV10C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware & Software Support for information on software/programming.

Parameter	Description	Typ	Max	Units
T_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	2.5	3.0	V

Input and I/O Pin Keeper

All ATF22V10C family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

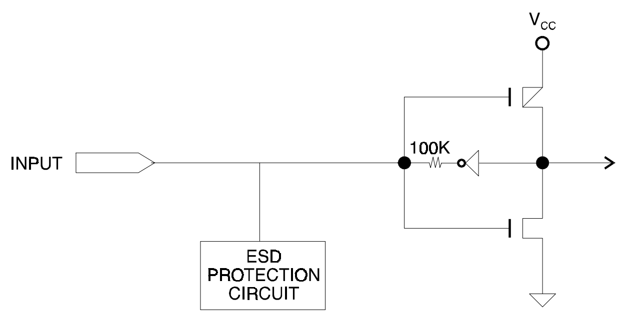
Power Down Mode

The ATF22LV10C includes an optional pin controlled power down feature. When this mode is enabled, the PD pin acts as the power down pin (Pin 4 on the DIP/SOIC packages and Pin 5 on the PLCC package). When the PD pin is high, the device supply current is reduced to less than 100 µA. During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in an undetermined state at the onset of power down will remain at the same state. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using the power down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

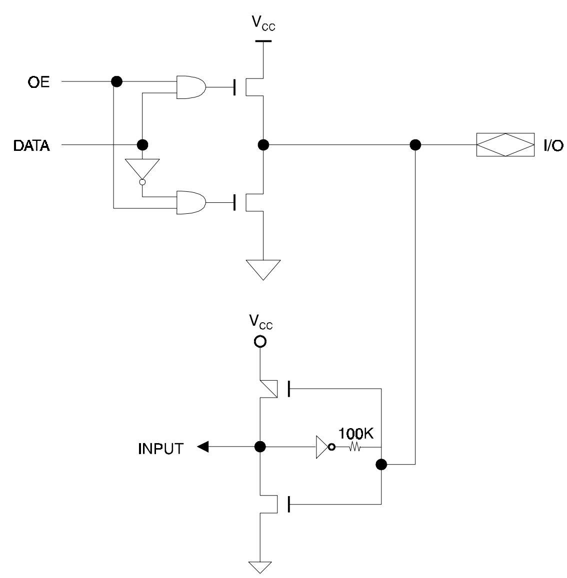
PD pin configuration is controlled by the design file, and appears as a separate fuse bit in the JEDEC file. When the power down feature is not specified in the design file, the IN/PD pin will be configured as a regular logic input.

Note: Some programmers list the 22V10 JEDEC compatible 22V10C (no PD used) separately from the non-22V10 JEDEC compatible 22V10CEX (with PD used).

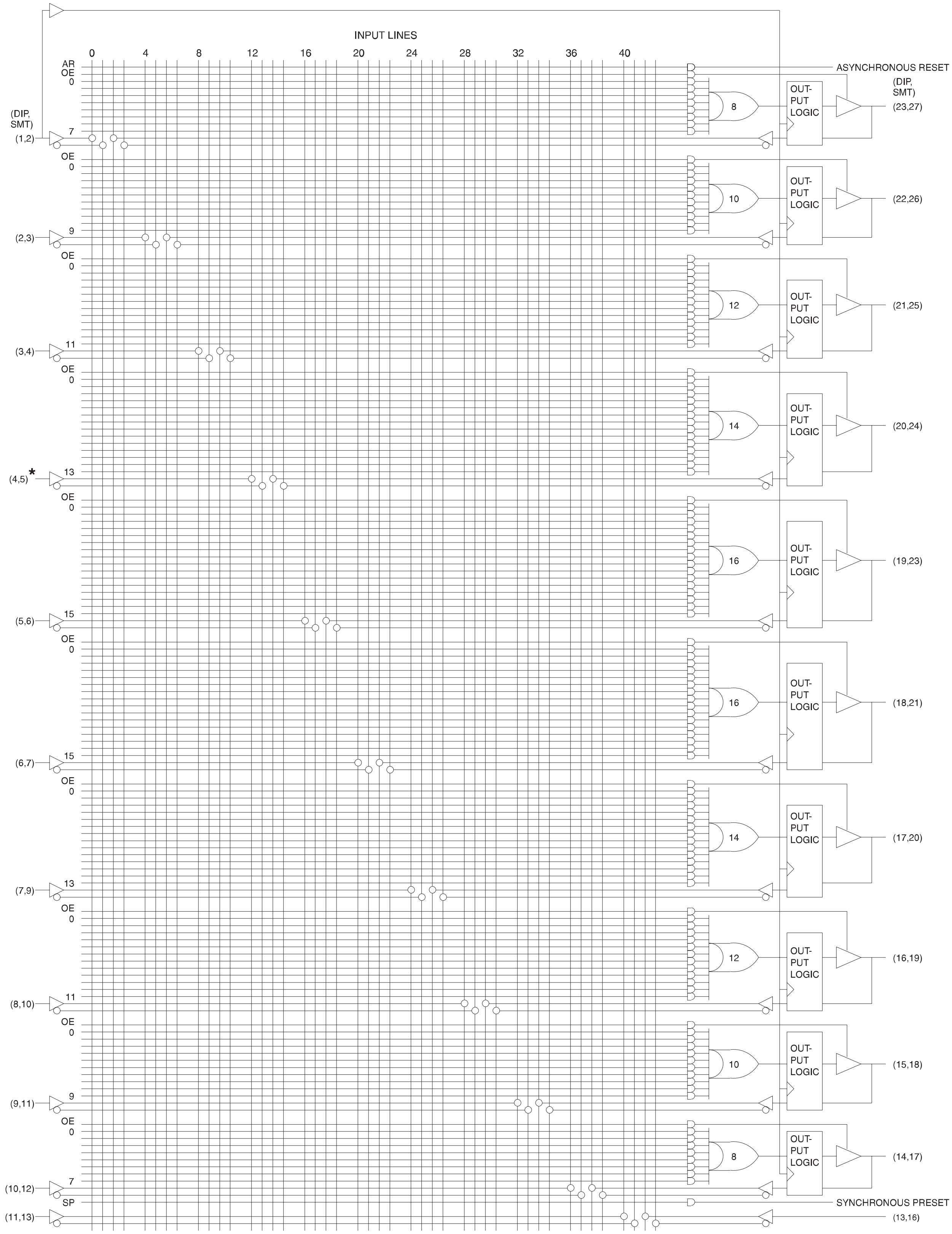
Input Diagram



I/O Diagram



Functional Logic Diagram ATF22LV10C



* Input not available if the power down (PD) option is utilized.

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7.5	6.5	ATF22LV10C-10JC ATF22LV10C-10PC ATF22LV10C-10SC ATF22LV10C-10XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
15	12	10	ATF22LV10C-15JC ATF22LV10C-15PC ATF22LV10C-15SC ATF22LV10C-15XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
	12	10	ATF22LV10C-15JI ATF22LV10C-15PI ATF22LV10C-15SI ATF22LV10C-15XI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)

Package Type	
28J	28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package (DIP)
24S	24-Lead, 0.300" Wide, Plastic Gull WIng Small Outline (SOIC)
24X	24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline TSSOP